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10/849,771	05/21/2004	Maxim Levit	42339-198286	9018

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	PAPER NUMBER
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/849,771	LEVIT, MAXIM	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/20/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-14,16-21 and 23-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-14, 16-21, 23-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to communications filed on 12/20/2006.

2. Claims 1, 10, 21, 24-26 have been amended, claims 27-29 have been added and claims 8, 15, 22 have been cancelled. Thus, claims 1-7, 9-14, 16-21, 23-29 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 6, 10, 11, 13, 17, 21, 23-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeddeloh et al (US Patent Application Publication 2006/0206738)

For claim 1, Jeddeloh et al teach the following limitations:

A device (Fig 5) comprising: a chip (504 is a memory module that comprises DRAM devices 104. [0003] mentions that the memory module is an SIMM. In that case each of 104 is a chip); means for measuring the temperature of the chip (370 measures the temperature of the chip as disclosed in [0028]); and means for regulating an operating voltage ([0034] mentions that 104 can be powered off to save power, which means stopping voltage) of the chip based on the measured temperature of the chip ([0024]

mentions that memory module is directed to reduced power state based on measured temperature) wherein when the sensed temperature of said means for measuring the temperature of the chip senses a chip temperature ([0029]) that is less than a predetermined threshold temperature value ([0029] mentions that 370 could be programmed to respond when temperature falls below a predetermined threshold) which represents an idle state of the chip ([0029] mentions that 370 signals 360 that 300 has not been actively used and could assume a reduced power state. 424 of Fig 4 labeled that state as idle temperature threshold. Therefore, this temperature represents idle state of the chip), said means for regulating the operating voltage of the chip changes the operating voltage of the chip to a minimum allowed value at its idle state (420; 420 can be stopping voltage as mentioned in [0034]. This is the minimum allowed value for the chips and the system since 312 and 360 are only powered to detect the command so that 104 and other dormant devices can be turned on as needed).

For claim 6, 360 is outside the chips and forms the external regulator.

For claim 27, threshold temperature represents idle state of the chip, which is an indication of reduced speed of the memory as mentioned in [0029] (i.e., memory module has not been actively used for a long time). Therefore, threshold temperature is based on speed characteristics of the chip at the threshold temperature. The minimum allowed voltage and threshold temperature maintain the reduced speed of the memory as long

as no memory command has been received while performing significant power reduction.

For claim 10, Jeddeloh et al teach the following limitations:

A device (Fig 5) **comprising: a chip** (504 is a memory module that comprises DRAM devices 104. [0003] mentions that the memory module is an SIMM. In that case each of 104 is a chip); **a thermometer that outputs the temperature of the chip** (370 measures the temperature of the chip as disclosed in [0028]); **and a voltage regulator** ([0034] mentions that 104 can be powered off to save power, which means stopping voltage, or regulating voltage. Thus, there is a voltage regulator. 360 is a part of voltage regulating circuitry as 360 is the component that direct the module to power down the memory chip) **coupled to the output of the thermometer** (360 is coupled to output of 370. 360 signals to power down the memory devices) **and to the chip** (360 is coupled to the chip) **wherein said voltage regulator reduces the operating voltage of the chip** (powered off comprises reducing voltage of the chip) **when the output of the thermometer is less than a threshold temperature** ([0029] mentions that 370 could be programmed to respond when temperature falls below a predetermined threshold) **representing an idle state of the chip** ([0029] mentions that 370 signals 360 that 300 has not been actively used and could assume a reduced power state. 424 of Fig 4 labeled that state as idle temperature threshold. Therefore, this temperature represents idle state of the chip) **and said voltage regulator reduces the operating voltage of the component to a minimum allowed voltage value in its idle state** (420; 420 can

be stopping voltage as mentioned in [0034]. This is the minimum allowed value for the chips and the system since 312 and 360 are only powered on to detect the command so that 104 and other dormant devices can be turned on as needed) **when the sensed temperature is below the threshold value** ([0024] mentions that memory module is directed to reduced power state based on measured temperature. [0029] mentions that 370 could be programmed to respond when temperature falls below a predetermined threshold).

For claim 11, SIMMs are semiconductor device.

For claim 13, 360 is outside the chips and forms the external regulator.

For claim 17, Jeddeloh teaches SIMM that is a card with chips and thermometer measures the temperature of the chips ([0028]) and regulator reduces the operating voltage of the chips ([0034]) when measured temperature is less than a threshold temperature ([0029]).

For claim 28, threshold temperature represents idle state of the chip, which is an indication of reduced speed of the memory as mentioned in [0029] (i.e., memory module has not been actively used for a long time). Therefore, threshold temperature is based on speed characteristics of the chip at the threshold temperature. The minimum allowed voltage and threshold temperature maintain the reduced speed of the memory as long

as no memory command has been received while performing significant power reduction.

For claim 21, Jeddeloh et al teach the following limitations:

A method, comprising: measuring the temperature of a chip while the chip is ON (412); **and reducing an operating voltage delivered to the chip** (420; [0034] mentions that 104 can be powered off, which comprises reducing voltage) **when the measured temperature of the chip drops below a predefined threshold temperature** ([0029] mentions that 370 could be programmed to respond when temperature falls below a predetermined threshold) **representing an idle state of the chip wherein the predefined threshold temperature is selected to be a chip temperature below which the chip is presumed to be in the idle state** ([0029] mentions that 370 signals 360 that 300 has not been actively used and could assume a reduced power state. 424 of Fig 4 labeled that state as idle temperature threshold. Therefore, this threshold temperature represents idle temperature of the chip).

For claim 23, chip returns to normal operating mode at 404.

For claim 29, threshold temperature represents idle state of the chip, which is an indication of reduced speed of the memory as mentioned in [0029] (i.e., memory module has not been actively used for a long time). Therefore, threshold temperature is based on speed characteristics of the chip at the threshold temperature. The minimum allowed

voltage and threshold temperature maintain the reduced speed of the memory as long as no memory command has been received while performing significant power reduction.

For claim 24, Jeddeloh et al teach the following limitations:

A machine-readable storage medium that provides instructions, which when executed by a computing platform, cause said computing platform to perform operations comprising a method of: measuring the temperature of a chip while the electrical chip is ON (412); **and reducing an operating voltage delivered to the chip** (420; [0034] mentions that 104 can be powered off, which comprises reducing voltage) **when the measured temperature of the chip drops below a predefined threshold temperature** ([0029] mentions that 370 could be programmed to respond when temperature falls below a predetermined threshold) **representing an idle state of the chip** ([0029] mentions that 370 signals 360 that 300 has not been actively used and could assume a reduced power state. 424 of Fig 4 labeled that state as idle temperature threshold. Therefore, this threshold temperature represents idle temperature of the chip).

For claim 25, threshold is the chip temperature below which chip is presumed to be an idle state as 424 labeled the threshold as an idle temperature threshold.

For claim 26, chip returns to normal operating mode at 404.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-5, 9, 12, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh et al (US Patent Application Publication 2006/0206738).

For claims 2 and 3, processor 202 is a semiconductor device (line 29 of column 4), which is typically Si based component.

For claims 4, 5, 12, Jeddeloh et al do not mention that the sensor is a thermocouple or thermal diode. Examiner takes an official notice that thermo couple and thermal diode is well known in the art. One ordinary skill in the art would have been motivated to use that particular sensor depending on his design choice.

For claims 9 and 16, 218 is not a firmware. Examiner takes an official notice that firmware storing data is well known in the art. One ordinary skill will be motivated to use firmware, since ROM is cheaper and provides non-volatile storage.

5. Claims 7, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh et al (US Patent Application Publication 2006/0206738), in view of Georgiou et al (US patent 6047248).

Jeddeloh et al do not teach any internal regulator. Georgiou et al teach an on-chip voltage regulator (Fig 1). One ordinary skill in the art would have been motivated to have an on-chip regulator to reduce the extra delay, since on-chip component takes less delay than off-chip component.

6. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over over Jeddeloh et al (US Patent Application Publication 2006/0206738), in view of Kikinis (US patent 5502838), further in view of Georgiou et al (US patent 6047248).

For claims 18 and 19, Jeddeloh teaches SIMM that is a card with chips and thermometer measures the temperature of the chips ([0028]) and regulator reduces the operating voltage of the chips ([0034]) when measured temperature is less than a threshold temperature ([0029]). Jeddeloh does not teach chip specific sensor and regulator. Kikinis teaches a system where each chip has sensor and the regulator regulates voltage of each chip (lines 5-10 of column 5 and lines 25-30 of column 5).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Jeddeloh and Kikinis. One ordinary skill in the art

would be motivated to have two chips with individual sensor and individual control of voltage, since that would increase the performance of the system.

The combined teachings of Jeddeloh and Kikinis does not teach chip specific regulator.

Georgiou et al teach the chip specific regulator (Fig 1).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Jeddeloh, Kikinis and Georgiou et al. One ordinary skill in the art would be motivated to have chip specific regulator, since that will increase the performance.

For claim 20, Examiner takes official notice that system comprising two regulators, where first regulator serves at least two chips and second regulator serving other chips are well known in the art. One ordinary skill would prefer such arrangement of regulators to ensure system's proper functionality.

Response to Arguments

Applicant's arguments filed on 12/20/2006 have been fully considered, but moot in view of new grounds of rejections.

The official notices used in action on 9/20/2006 are considered as admitted prior art, since they are not traversed by the applicant.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fahmida Rahman

Examiner

Art Unit 2116

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THUAN N. DU
PRIMARY EXAMINER